34556/JFO/B600

CLAIMS

What is claimed is:

1. A memory structure, comprising:

a. an Address Resolution Table for resolving addresses in a packet-based network switch; and

b. a Packet Storage Table, the Packet Storage Table adapted to receive a packet for storage in the packet-based network switch, and sharing a preselected portion of memory with the Address Resolution Table.

2. The memory structure of claim 1, further comprising at least one of:

a. a Transmit Descriptor Table being associated with a corresponding packet-based network transmit port; and

b. a Free Buffer Pool having plural memory buffers, each of the plural memory buffers having a pre-determined number of memory locations associated therewith.

3. The memory structure of claim 1 wherein the packet-based network switch implements an IEEE Standard 802.3 communication protocol.

4. The memory structure of claim 3 wherein the switch comprises plural ports.

5. The memory structure of claim 4 wherein the switch comprises at least 8 ports.

6. The memory structure of claim 1 wherein the associative memory structure comprises one of an ***n***-way associative memory, a hash table, a binary search structure, and a sequential search structure.

7. The memory structure of claim 3 wherein the number of memory accesses required per Ethernet frame is one of:

a. one cycle per frame for address resolution;
b. one cycle per frame for address learning;
c. one cycle per frame for transmission read;
d. one cycle per frame for transmission write;
e. one cycle per eight bytes for a frame data read; and
f. one cycle per eight bytes for a frame data write.

8. A memory structure comprising an Address Resolution Table having an associative memory structure, the Address Resolution Table for resolving addresses in a packet-based network switch.

9. The memory structure of claim 8 further comprising a Packet Storage Table, the Packet Storage Table adapted to receive at least one of each of a Packet Data Address and a Packet Data Value.

10. The memory structure of claim 9 further comprising a Transmit Descriptor Table, the Transmit Descriptor Table being associated with a corresponding packet-based network transmit port, and the Transmit Descriptor Table adapted to receive a Table Descriptor Address and a Table Descriptor Value.

11. The memory structure of claim 8 wherein the associative memory structure comprises one of a direct-mapped/one-way associative memory structure and a two-way associative memory structure.

12. The memory structure of claim 11 wherein the number of memory accesses required per Ethernet frame is one of:

a. one cycle per frame for address resolution;

b. one cycle per frame for address learning;

c. one cycle per frame for transmission read;

d. one cycle per frame for transmission write;

e. one cycle per eight bytes for a frame data read; and

f. one cycle per eight bytes for a frame data write.

13. A memory structure having a memory block, the memory block comprising at least two of:

a. an Address Resolution Table having an associative memory structure, the Address Resolution Table for resolving addresses in a packet-based network switch;

b. a Transmit Descriptor Table, the Transmit Descriptor Table being associated with a corresponding packet-based network transmit port, and the Transmit Descriptor Table adapted to receive a Table Descriptor Address and a Table Descriptor Value; and

c. a Packet Storage Table, the Packet Storage Table adapted to receive at least one of each of a Packet Data Address and a Packet Data Value.

14. The memory structure of claim 13 wherein the associative memory structure comprises one of an ***n***-way associative memory, a hash table, a binary search structure, and a sequential search structure.

15. The memory structure of claim 13 wherein the memory block comprises a shared memory block.

16. The memory structure of claim 13 wherein the Transmit Descriptor Table comprises a FIFO memory structure.

17. The memory structure of claim 16 wherein the FIFO memory structure comprises a circular FIFO memory structure, the FIFO memory structure having a head memory pointer and a tail memory pointer.

18. The memory structure of claim 13 further comprising a Free Buffer Pool having plural memory buffers, each of the plural memory buffers having a pre-determined number of memory locations associated therewith.

19. The memory structure of claim 18, wherein the Free Buffer Pool further comprises a buffer control memory.

20. The memory structure of claim 19, wherein the free buffer pool control memory comprises plural memory bits, ones of the plural data bits uniquely corresponding to ones of the pre-determined number of buffer pool memory locations.

21. The memory structure of claim 18, wherein at least two of the Address Resolution Table, the Transmit Descriptor Table, the Packet Storage Table, and the Free Buffer Pool share a memory block.

22. The memory structure of claim 21 wherein the number of memory accesses required per Ethernet frame is one of:

a. one cycle per frame for address resolution;

b. one cycle per frame for address learning;

c. one cycle per frame for transmission read;
d. one cycle per frame for transmission write;
e. one cycle per eight bytes for a frame data read; and
f. one cycle per eight bytes for a frame data write.

23. The memory structure of claim 18, further comprising a free buffer manager, including:
a. a buffer bus controller;
b. a buffer bus register;
c. a buffer control finite state machine, operably coupled with the bus controller and the bus register; and
d. a buffer search engine, operably coupled with the bus controller, bus register, and finite state machine.

24. The memory structure of claim 23 wherein the buffer bus controller comprises:
a. a buffer free bus controller for detecting a buffer request and present the request to at least one of the finite state machine and the buffer search engine; and
b. a buffer grant bus controller for granting an available free buffer, as indicated by the buffer bus register.

25. The memory structure of claim 23 wherein the buffer search engine comprises a pipelined buffer search engine.

26. The memory structure of claim 23 wherein the buffer bus register comprises a LIFO.

27. The memory structure of claim 26 wherein the LIFO comprises an eight-location LIFO.

28. A packet-based switch comprising a shared memory structure having a Address Resolution Table and a Packet Storage Table.

29. The packet-based switch of claim 28 wherein the switch implements an IEEE Standard 802.3 communication protocol.

30. The packet-based switch of claim 29 wherein the switch comprises plural ports.

31. The packet-based switch of claim 28 wherein the number of memory accesses required per Ethernet frame is one of:

a. one cycle per frame for address resolution;
b. one cycle per frame for address learning;
c. one cycle per frame for transmission read;
d. one cycle per frame for transmission write;
e. one cycle per eight bytes for a frame data read; and
f. one cycle per eight bytes for a frame data write.

32. A packet-based switch having a memory structure, the memory structure comprising at least two of:

a. an Address Resolution Table having an associative memory structure, the Address Resolution Table for resolving addresses in a packet-based network switch;

b. a Transmit Descriptor Table, the Transmit Descriptor Table being associated with a corresponding packet-based network transmit port, and the Transmit Descriptor Table adapted to receive a Table Descriptor Address and a Table Descriptor Value; and

c. a Packet Storage Table, the Packet Storage Table adapted to receive at least one of each of a Packet Data Address and a Packet Data Value.

33. The packet-based switch of claim 32, wherein the associative memory structure comprises one of an ***n***-way associative memory, a hash table, a binary search structure, and a sequential search structure.

34. The packet-based switch of claim 32 wherein the memory block comprises a shared memory block.

35. The packet-based switch of claim 32 wherein the Transmit Descriptor Table comprises a FIFO memory structure.

36. The packet-based switch of claim 35 wherein the FIFO memory structure comprises a circular FIFO memory structure, the FIFO memory structure having a head memory pointer and a tail memory pointer.

37. The packet-based switch of claim 32 further comprising a Free Buffer Pool having plural memory buffers, each of the plural memory buffers having a pre-determined number of memory locations associated therewith.

38. The packet-based switch of claim 37, wherein the Free Buffer Pool further comprises a buffer control memory.

39. The packet-based switch of claim 38, wherein the free buffer pool control memory comprises plural memory bits, ones of the plural data bits uniquely corresponding to ones of the pre-determined number of buffer pool memory locations.

40. The packet-based switch of claim 37, wherein at least two of the Address Resolution Table, the Transmit Descriptor Table, the Packet Storage Table, and the Free Buffer Pool share a memory block.

41. The packet-based switch of claim 34 wherein the number of memory accesses required per Ethernet frame is one of:

a. one cycle per frame for address resolution;

b. one cycle per frame for address learning;

c. one cycle per frame for transmission read;

d. one cycle per frame for transmission write;

e. one cycle per eight bytes for a frame data read; and

f. one cycle per eight bytes for a frame data write.

42. The packet-based switch of claim 38, further comprising a free buffer manager, including:

a. a buffer bus controller;

b. a buffer bus register;

c. a buffer control finite state machine, operably coupled with the bus controller and the bus register; and

d. a buffer search engine, operably coupled with the bus controller, bus register, and finite state machine.

43. The packet-based switch of claim 42 wherein the buffer bus controller comprises:

a. a buffer free bus controller for detecting a buffer request and present the request to at least one of the finite state machine and the buffer search engine; and

b. a buffer grant bus controller for granting an available free buffer, as indicated by the buffer bus register.

44. The packet-based switch of claim 42 wherein the buffer search engine comprises a pipelined buffer search engine.

45. The packet-based switch of claim 42 wherein the buffer bus register comprises a LIFO.

46. The packet-based switch of claim 45 wherein the LIFO comprises an eight-location LIFO.

47. The packet-based switch of claim 33 wherein the switch implements an IEEE Standard 802.3 communication protocol.

48. The packet-based switch of claim 47 wherein the switch comprises plural ports.

49. The packet-based switch of claim 47 wherein the switch comprises at least 4 ports.

50. The packet-based switch of claim 47 wherein the switch comprises at least 8 ports.

51. The packet-based switch of claim 45 wherein the number of memory accesses required per Ethernet frame is one of:

a. one cycle per frame for address resolution;
b. one cycle per frame for address learning;
c. one cycle per frame for transmission read;
d. one cycle per frame for transmission write;
e. one cycle per eight bytes for a frame data read; and
f. one cycle per eight bytes for a frame data write.

52. A packet-based switch comprising an Address Resolution Table having a one-way associative memory structure and a Packet Data Buffer Table sharing a memory block with the Address Resolution Table.

53. The packet-based switch of claim 52 wherein the switch comprises plural ports.

54. The packet-based switch of claim 52 wherein the switch comprises at least 4 ports.

55. The packet-based switch of claim 52 wherein the switch comprises at least 8 ports.

56. The packet-based switch of claim 52 wherein the number of memory accesses required per Ethernet frame is one of:

a. one cycle per frame for address resolution;
b. one cycle per frame for address learning;
c. one cycle per frame for transmission read;
d. one cycle per frame for transmission write;
e. one cycle per eight bytes for a frame data read; and
f. one cycle per eight bytes for a frame data write.

57. A packet-based switch, comprising an Address Resolution Table having a direct-mapped/one-way associative memory structure, the Address Resolution Table for resolving addresses in a packet-based network switch.

58. The packet-based switch of claim 58 wherein the direct-mapped/one-way associative memory is searched using a destination address key direct-mapped address search.

59. The packet-based switch of claim 58 wherein the switch implements an IEEE Standard 802.3 communication protocol.

60. The packet-based switch of claim 59, wherein the switch comprises plural ports.